A fully integrated continuous-time 1Hz low-pass filter with high dynamic range and low distortion

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A fully integrated continuous-time 1Hz low-pass filter with high dynamic range and low distortion

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Abstract

A first order 1Hz integrated filter needing no external components is described. It uses an on-chip capacitor of 100pF and a new differential transconductance amplifier which allows direct implementation of very small transconductances by using MOS transistors in their triode region. This furthermore makes the filter cutoff frequency electrically adjustable. The distortion is very low, less than 0.1% at $4V_{pp}$ input voltage. Also the signal-to-noise ratio is good, more than 80dB at 0.1% distortion. This is remarkable because the well-known high *1/f*-noise level of MOS transistors is particularly severe at the very low frequencies of interest here.

Introduction

The implementation of very low frequency continuous-time filters in integrated circuits poses a challenge because on-chip capacitors are limited to quite low values in order not to consume excessive silicon area. As an example, if a 1Hz first order lowpass filter is implemented as a simple *RC* stage and the capacitor is chosen as $C=100\text{pF}$ then the resistor has to be $R=1.59\text{G}\Omega$. Clearly, such a resistor would occupy a vast area if it were implemented directly by using some resistive layer of a standard IC fabrication process. Consequently, the resistances needed have to be realized by other means, or special circuit techniques must be used to achieve the desired very large time constants without needing large capacitors or resistances [1]. This paper uses a combination of the two approaches, introducing a new transconductance amplifier with very low transconductance and using a current mirror to scale down the transconductor output current, thus further lowering the transconductance. A very large time constant integrator is formed by feeding the output current into a capacitor of 100pF and this is used as the basic building block in a 1Hz first order lowpass filter.

A new transconductor with very small transconductance

The transconductor is based on MOS transistors operating in the triode region. Here, the current-to-voltage relationship is approximately given as:

$$I = K\frac{W}{L}V_{DS}(V_{GS}-V_T-\tfrac{1}{2}V_{DS}) \quad \text{for } V_{DS}<V_{GS}-V_T \tag{1}$$

where K is the process current factor. By letting V_{DS} be constant, a linear transfer from gate-source voltage to drain current is obtained and the transconductance is:

$$g_m = K\frac{W}{L}V_{DS} \tag{2}$$

Accordingly, by using a small value of V_{DS}, a small transconductance value is obtained.

The constant drain-source voltage can be brought about very simply by cascoding or, better, by using a modification of the socalled "Regulated Cascode" (RGC) structure [2] as shown in Figure 1. Since the current through M2 is constant V_{GS2} is also constant and $V_{DS1} = V_{GS2} - V_1$. Furthermore, due to the gain enhanced cascoding the output impedance is extremely high, thus enabling direct connection to high-impedance loads such as capacitors.

In addition to the linear transfer, (1) also contains an undesired constant term. This is, however, easily removed by using a differential configuration as shown in Figure 2 (here, p-channel transistors are used in order to be in agreement with the experimental circuit). With the shown biasing arrangement, transistors M2A, M2B, and M4 all conduct a constant current of I_{Bias1}, thus producing a constant drain source voltage of $V_{DS1} = \sqrt{2I_{bias1}}\,(1/\sqrt{KW_2/L_2} - 1/\sqrt{KW_4/L_4})$ across the actual transconductance transistors M1A and M1B. The quiescent current through each of these is then $\frac{1}{2}I_{Bias2}$.

M1A and M1B will usually be very long and hence have a large gate area. Consequently, even at quite low frequencies the current through the resulting gate-drain and gate-source capacitances can exceed the desired (but very small) transconductance current. Due to symmetry, the gate-source currents of M1A and M1B will cancel each other but the gate-drain currents add directly to the output currents, thus introducing a right half plane zero in the transfer characteristic. Therefore, a feedforward compensation, MC1A and MC1B, has been introduced. These two transistors are half the length of M1A and M1B and do thereby function as capacitors of approximately the same value as the gate-drain capacitances of M1A and M1B. Consequently, by applying opposite gate voltages to M1A and MC1A the gate-drain current of M1A is cancelled by the gate-drain current of MC1A. Similarly for M1B and MC1B.

The bias current I_{Bias2} is generated by the circuit shown in Figure 3. This is essentially just a replica of one half of the transconductor. By applying a desired quiescent voltage at the V_{IQ} terminal a corresponding current will flow through M1C and this is then copied to the transconductor by the $1{:}A$ current mirror. To account for the two branches in the transconductor A must be 2. Alternatively, V_{IQ} can be shorted to V_{SS} and A set to 1. In the transconductor this corresponds to a situation with maximum differential input voltage and, consequently, a bias current results which ensures maximum dynamic range.

Apart from cancelling a constant term, the differential configuration also increases the dynamic range because the maximum signal level is doubled. Also, distortion is lowered because the balancing cancels the remaining even order distortion, leaving only odd order distortion. Furthermore, due to symmetry, the V_{CMreg} terminal in Figure 2 reflects the common-mode value of the input voltage and can therefore be used to form a common-mode feedback loop as we shall see below. It is also worth noting that, contrary to most other differential schemes, mismatch only leads to an offset, not to (severely) increased distortion. This is because each half of the differential circuit is linear in itself.

In comparison with the well-known MOSFET-C [3] technique the new transconductor allows very small drain-source voltages, thereby enabling implementation of small transconductances without needing excessive L/W ratios - the (trans)conductance of the MOSFET-C technique is fundamentally limited to be larger than $KW/L \cdot V_{max}$ where V_{max} is the maximum input voltage swing [3]. On the other hand, the MOSFET-C technique has the advantage that no DC current flows through the MOS transistors, thereby eliminating *1/f*-noise. Also, the new transconductor is rather sensitive to noise on the assumed constant drain-source voltage because the small signal transfer from the drain-source voltage to the output current is $g_d = KW/L(V_{GS} - V_T - V_{DS})$ which normally will be significantly larger than the g_m of (2). Hence, M2A and M2B (but not M4) will be important noise contributors and their area should consequently be made large (the *1/f*-noise power is inversely proportional to gate area [4, chapter 11]). If a BiCMOS technology is available, the combination of M2A, M2B and M4 should be replaced by low noise bipolar circuitry. M3A and M3B should remain MOS transistors because their only noise contribution, the gate current noise, is virtually zero at the very low frequencies of interest.

Filter implementation and experimental results

The filter is based on an integrator and is implemented as shown in Figure 4. The transconductors have a transconductance of $I_{out2} - I_{out1} = (159\text{M}\Omega)^{-1}(V_{in1} - V_{in2})$ and by the current mirrors (M6A,M6B) and (M7A,M7B) this is further lowered by a factor 10 to obtain the desired transconductance of $(1.59\text{G}\Omega)^{-1}$. Transistors M8A and M8B function as current sources to supply quiescent current. To obtain a well-defined output common-mode voltage the sum of their currents must exactly match the sum of the currents in M6B and M7B. This is ensured by the extremely simple common-mode feedback scheme consisting of simply connecting the gates of M8A and M8B to the already existing V_{cmreg} terminal of one of the transconductors. The transistor sizes are listed in Table I and the nominal quiescent current I_{bias1} is

100nA. The chip was laid out in ALCATEL-MIETEC's 2.4μm CMOS process; a photo is shown in Figure 5.

The measured frequency response of the filter is shown in Figure 6, both with and without feedforward compensation. Clearly, the compensation greatly improves the response, moving the parasitic zero from 7kHz to at least 20kHz. Also it has been verified by measurements that the compensation does not change the distortion properties significantly. To achieve a fair measure of the distortion the dominant harmonics must not be attenuated by the filter response. Therefore a 0.25Hz sine voltage was chosen in the measurements. The measurements results are summarized below (distortion measurements for $V_{in}<3V_{pp}$ were not possible because the sine generator itself had a harmonic distortion of 0.03%):

Power supply:	±5V
Output noise voltage (0.023-6.25Hz):	146μVRMS
Harmonic distortion at $V_{in}=3V_{pp}$:	<0.04%
Harmonic distortion at $V_{in}=4V_{pp}$:	<0.1%
Signal-to-noise ratio:	>80dB

This gives a S/N ratio of more than 80dB at 0.1% distortion. The measured power spectral density of the noise is shown in Figure 7, clearly indicating that *1/f*-noise is dominant.

Conclusion

It has been demonstrated that very low frequency continuous-time filters with high dynamic range and low distortion are feasible in CMOS technology. A signal-to-noise ratio of 80dB at 0.1% distortion was achieved experimentally and it has been outlined how even better performance could be obtained by careful design of certain transistors (M2A and M2B) or by using a BiCMOS technology.

References

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[3] Y. P. Tsividis, M. Banu, and J. Khoury, *Continuous-Time MOSFET-C Filters in VLSI*, IEEE Transactions on Circuits and Systems, vol. CAS-33, no. 2, February 1986.

[4] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, Wiley 1984.

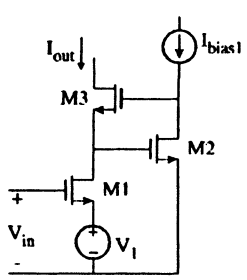

Figure 1 Simple transconductor using a regulated gain cascode.

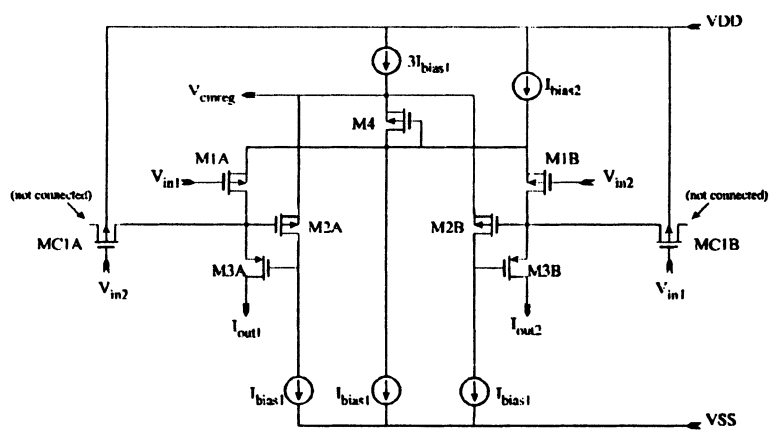

Figure 2 Differential transconductor with very small transconductance.

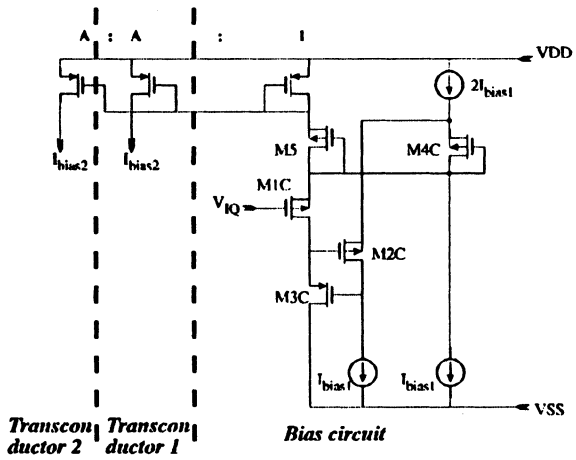

Figure 3 Bias circuit. The mirror ratio A is either 1 or 2.

Transistor	W/L [μm/μm]
M1A/B/C	4/678
M2A/B/C	4.8/44
M3A/B/C	33.6/6
M4/C	4.8/22.4
M5	9.6/2.4
M6A/M7A	4/114
M6B/M7B	4/1140
M8A/B	4/253

Table I Transistor sizes.

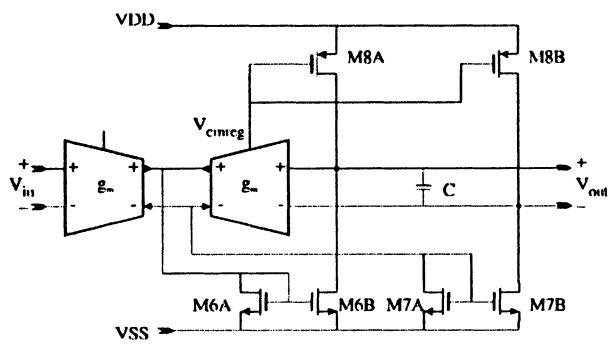

Figure 4 Schematic of the filter. The transconductors are shown in Figure 2.

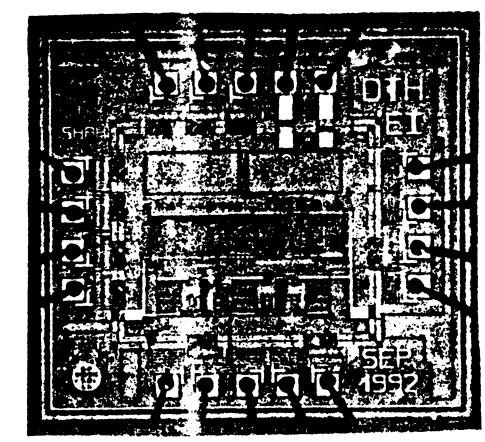

Figure 5 Chip photo. The actual filter (i.e. excluding output buffers) measures 1.3mm × 0.8mm.

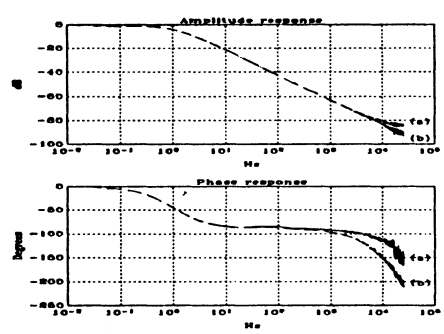

Figure 6 Amplitude and phase response of the filter with (a) and without (b) feed-forward compensation.

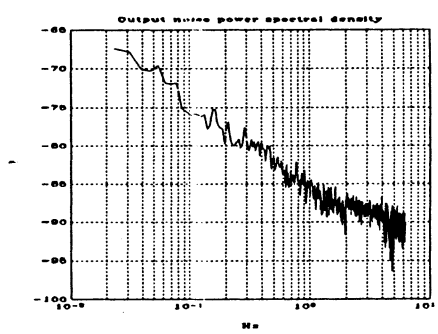

Figure 7 Power spectral density of the output voltage noise.